WHAT IS CLAIMED IS:

SUB B1

1. A semiconductor device, in which a multi-layered insulation film is formed on a semiconductor substrate and wires are formed in said multi-layered insulation film, characterized in that said multi-layered insulation film comprises a first insulation layer composed of an organic material having low dielectric constant which has a lower dielectric constant than silicon oxide, a second insulation layer composed of a polysiloxane compound having an Si-H group and formed on and being in contact with a top of said first insulation layer, and a third insulation layer composed of an inorganic material and formed on and being in contact with a top of said second insulation layer.

2. The semiconductor device according to claim 1, characterized in that said first insulation layer is composed of an organopolysiloxane or aromatic-containing organic resin.

3. The semiconductor device according to claim 1, characterized in that said second insulation layer is composed of hydrogen silisesquioxane and/or hydride organosiloxane.

4. The semiconductor device according to claim 1, characterized in that said third insulation layer is composed of one or more materials selected from the group consisting of silicon oxide, silicon nitride and silicon oxynitride.

SUB B'

5. A semiconductor wafer with a multi-layered insulation film formed on one surface of the wafer, characterized in that said multi-layered insulation film comprises a first insulation layer composed of an organic material of low dielectric constant which has a lower dielectric constant than silicon oxide, a second insulation layer composed of a polysiloxane compound having an Si-H group and formed on and being in contact with a top of said first insulation layer, and a third insulation layer composed of an inorganic material and formed on and being in contact with a top of said second insulation layer.

6. The semiconductor wafer according to claim 5, characterized in that said first insulation layer is composed of an organopolysiloxane or aromatic-containing organic resin.

7. The semiconductor wafer according to claim 5, characterized in that said second insulation layer is composed of hydrogen silisesquioxane and/or hydride organosiloxane.

8. The semiconductor wafer according to claim 5, characterized in that said third insulation layer is composed of one or more materials selected from the group consisting of silicon oxide, silicon nitride and silicon oxynitride.

9. A method of forming a multi-layered insulation film on a semiconductor wafer, the multi-layered insulation film containing a first insulation layer, a second insulation layer and a third insulation layer, characterized in that

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the method comprises the steps of forming the first insulation layer composed of an organic material of low dielectric constant which has a lower dielectric constant than silicon oxide, forming the second insulation layer composed of a polysiloxane compound having an Si-H group such that the second insulation layer is in contact with a top of the first insulation layer, and forming the third insulation layer composed of an inorganic material such that the third insulation layer is in contact with a top of the second insulation layer.

10. The method of forming a multi-layered insulation film according to claim 9, characterized in that said first insulation layer is composed of an organopolysiloxane or aromatic-containing organic resin.

11. The method of forming a multi-layered insulation film according to claim 9, characterized in that said second insulation layer is composed of hydrogen silisesquioxane and/or hydride organosiloxane.

12. The method of forming a multi-layered insulation film according to claim 9, characterized in that said third insulation layer is composed of one or more materials selected from the group consisting of silicon oxide, silicon nitride and silicon oxynitride.

13. The method of forming a multi-layered insulation film according to claim 9, characterized in that said first and second insulation layers are formed by the plasma CVD

method without taking out semiconductor wafer from the plasma atmosphere.

14. The method of forming a multi-layered insulation film according to claim 13, characterized in that a feed gas for forming said first insulation layer is a mixed gas containing alkylsilane gas and oxidizing gas, and a feed gas for forming said second insulation layer is a mixed gas containing monosilane gas, alkylsilane gas and oxidizing gas.

15. The method of forming a multi-layered insulation film according to any one of claims 9 to 12, characterized in that said semiconductor wafer is spin-coated with a solution containing said organic material of low dielectric constant and then thermally treated to form said first insulation layer, and said first insulation layer is thermally treated in atmosphere at 200°C or more, and 500°C or less, inclusive, and coated with said second insulation layer by plasma CVD method.

16. A method of producing a semiconductor device, characterized in that the method comprises steps of forming a first insulation layer composed of an organic material of low dielectric constant which has a lower dielectric constant than silicon oxide, on a semiconductor substrate; forming a second insulation layer composed of a polysiloxane compound having an Si-H group such taht the second insulation layer is in contact with a top of said first insulation layer; forming a third insulation layer composed of an inorganic

material such that the third insulation layer is in contact with a top of said second insulation layer; etching said first, second and third insulation layers to form recesses therein; forming an electroconductive film over the entire surfaces of said recesses in such a way to fill them; and removing said electroconductive film formed on the region outside of each of said recesses by chemical mechanical polishing or etching.

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17. A method of producing a semiconductor device characterized in that the method comprises steps of: forming, on a semiconductor substrate, a gate electrode with a side-wall insulation layer provided on its side, and a pair of impurity diffusion regions in the surface area of the semiconductor substrate on both sides of the gate electrode; forming a first insulation layer composed of an organic material of low dielectric constant which has a lower dielectric constant than silicon oxide, over the entire surface; forming a second insulation layer composed of a polysiloxane compound having an Si-H group such that the second insulation layer is in contact with a top of said first insulation layer; forming a third insulation layer composed of an inorganic material such that the third insulation layer is in contact with a top of said second insulation layer; etching said first, second and third insulation layers to form a contact hole, exposing said impurity diffusion regions to the bottom of said contact hole, and exposing said side-wall insulation layer to the side of said contact hole;

and forming an electroconductive film over the entire surface in such a way to fill said contact hole.

18. The method of producing a semiconductor device according to claim 16, characterized in that said first insulation layer is composed of an organopolysiloxane or aromatic-containing organic resin.

19. The method of producing a semiconductor device according to claim 16, characterized in that said second insulation layer is composed of hydrogen silisesquioxane and/or hydride organosiloxane.

20. The method of producing a semiconductor device according to claim 16, characterized in that said third insulation layer is composed of one or more materials selected from the group consisting of silicon oxide, silicon nitride and silicon oxynitride.

21. The method of producing a semiconductor device according to claim 16, characterized in that said first and second insulation layers are formed by the plasma CVD method without taking out said semiconductor wafer from the plasma atmosphere.

22. The method of producing a semiconductor device according to claim 21, characterized in that the feed gas for forming said first insulation layer is a mixed gas containing alkylsilane gas and oxidizing gas, and the feed gas for forming said second insulation layer is a mixed gas containing monosilane gas, alkylsilane gas and oxidizing gas.

Sub A4

23. The method of producing a semiconductor device according to any one of claims 16 to 20, characterized in that said semiconductor wafer is spin-coated with a solution containing the organic material of low dielectric constant and then thermally treated to form said first insulation layer, and said first insulation layer is thermally treated in atmosphere at 200°C or more and 500°C or less, inclusive, and coated with said second insulation layer by plasma CVD method.

Add A5

Add B2